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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,899	06/29/2000	Alain Benayoun	FR9-1999-0027-US1	7629

7590 04/05/2004

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EXAMINER	
LIN, KENNY S	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 04/05/2004

10

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,899	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Kenny Lin	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Blelloch et al (hereinafter Blelloch), US 6,434,590.

4. As per claim 1, Blelloch taught the invention as claimed including a hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a

number of processes some of which are dependant on binary decisions (col.2, lines 29-60) said device comprising:

a. A plurality of task units for processing data, making decisions and/or processing data and making decisions (col.2, lines 45-46);

b. A task interconnection logic means interconnecting the task units for communicating actions from a source task unit to a destination task unit (col.2, lines 46-55, 61-67, col.3, lines 1-8, 10-15, an interconnection logic means is inherently needed in communicating between source task unit and destination task units).

c. Each of said task units including a processor for executing the steps of the associated task in response to a received request action (col.2, lines 46-55); and,

d. A status manger for handling actions from source task units and building actions to be sent to destination task units (col.2, lines 43-48).

5. As per claim 11, Blelloch taught the invention as claimed in claim 1. Blelloch further taught wherein each task unit of the plurality of task units is configured to perform only one task of the plurality of tasks associated with the algorithm.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-3, 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch, US 6,434,590.

8. As per claim 12, Blelloch a hardware device for concurrently processing a plurality of tasks associated with an algorithm (col.2, lines 29-60), comprising:

a. At least two task units each configured to process the steps of a respective single task of a multiple task algorithm (col.2, lines 45-46);

b. At least two processors configured to execute the respective single task in each of the respective at least two task units (col.2, lines 45-46);

c. An interconnection logic means for routing actions from a source task unit to a destination task unit of the at least two task units, respectively (col.2, lines 30-32, fig.1); and

d. A status managers being associated with each of the at least two task units (col.2, lines 43-51).

9. Blelloch taught to use one status manager in associating with the task units in the processing system (col.2, lines 43-60) where the status manager receive actions from the interconnection logic means and directing execution of the single task (col.2, lines 52-55). Blelloch did not specifically teach at least two status managers each being associated with each of the at least two task units, respectively. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the need of having more

than one status managers and lower the cost of device since the one status manager taught in Blelloch's device is able to perform the same desired needs of having multiple status managers.

10. As per claim 2, Blelloch taught the invention substantially as claimed in claim 1. Blelloch further taught that wherein said actions communicated form a source task unit to a destination task unit are START used to activate the processor of said destination task unit (col.2, lines 52-55) and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said task (col.3, lines 26-27). Blelloch did not specifically teach the actions to include KILL used to cancel the task associated with said destination task unit. However, it would have been obvious to add different actions to perform desired actions according to administrating needs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Papadopoulos's system with actions such as KILL and PAUSE to perform administrative actions.

11. As per claim 3, Blelloch taught the invention substantially as claimed in claim 2. Blelloch further taught that wherein said status manager activates said processor for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START (col.2, lines 61-67, col.3, line 1).

12. As per claim 13, Blelloch taught the invention substantially as claimed in claim 12. Blelloch further taught wherein each of the task units repetitively perform only its respective single task (col.2, lines 55-57).

13. As per claim 14, Blelloch taught the invention substantially as claimed in claim 13. Blelloch further taught that wherein the status manager handles incoming commands for other task units of the at least two task units and builds commands to be sent to one of the other task units (col.2, lines 43-48).

14. As per claim 15, Blelloch taught the invention substantially as claimed in claim 14. Blelloch further taught wherein the source task unit is configured to activate the destination task unit (col.2, lines 30-32, 38-48).

15. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch as applied to claims 1-3 above, and further in view of Papadopoulos et al (hereinafter Papadopoulos), US 5,430,850.

16. Papadopoulos was cited in the previous office action.

17. As per claim 4, Blelloch taught the invention substantially as claimed in claim 3. Blelloch did not specifically teach that the wherein said status manager is a state machine. Papadopoulos taught that the status manager is a state machine (col.26, lines 54-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Papadopoulos because Papadopoulos' teaching of using a state machine as the status manager enables the status manager in Blelloch's device to consume messaging abilities.

18. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch as applied to claims 1-3 above, and further in view of Papadopoulos et al (hereinafter Papadopoulos), US 5,430,850 and "Official Notice".

19. As per claim 5, Blelloch taught the invention substantially as claimed in claim 3. Blelloch did not specifically teach that wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow (col.5, lines 24-39). Papadopoulos taught that wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow (col.5, lines 24-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Papadopoulos because Papadopoulos' teaching of having a plurality of control/data register in the task units provides Blelloch's device address registration abilities. Blelloch and Papadopoulos did not specifically teach that each one of said control/data registers comprising a control field composed of a completion bit set to 1 when the associated task is completed, a validation bit set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision. However, Official Notice is taken that both the concept and advantage of using bits in data register is well known and expected in the art. It would have been obvious to use bits in data register to indicate the condition of the associated task. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use specific bit(s) to indicate the status of the task in Blelloch and Papadopoulos' system according to design choice.

20. As per claim 6, Blelloch and Papadopoulos taught the invention substantially as claimed in claim 5. Blelloch and Papadopoulos did not specifically teach that wherein each of said control/data registers includes a data field which is loaded if necessary by said status manager activated by an action received form a source task unit, said processor using these data for executing the task associated with said task unit and replacing them if necessary. However, Official Notice is taken that it would have been obvious to load a data field or execute any job when an action is received. It would have been obvious to one of ordinary skill in the art at the time the invention was made to load a data field by the status manager in Blelloch and Papadopoulos's system when the status manager receives an action commanding to do so.

21. As per claim 7, Blelloch and Papadopoulos taught the invention substantially as claimed in claim 6. Blelloch and Papadopoulos did not specifically teach that wherein said completion bit is sent by said processor to said status manager after completion of the task execution. However, Official Notice is taken that both the concept and advantage of using notification is well known and expected in the art. It is obvious to send notifications to notify the status manager of the current status. It would have been obvious to one of ordinary skill in the art at the time the invention was made to send a completion bit to the status manager in Blelloch and Papadopoulos' system to notify the completion of task execution in the system.

22. As per claim 8, Blelloch and Papadopoulos taught the invention substantially as claimed in claims 5-7. Blelloch and Papadopoulos did not specifically teach that wherein said control/data register corresponding to a specific instance is cleared by said status manager when

this one receives an action KILL for the task associated with said task unit and for said specific instance. However, Official Notice is taken that both the concept and advantage of using a KILL/Delete action is well known and expected in the art. It would have been obvious that the objective of a KILL/Delete action is to remove a specific instance. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a KILL action in Blelloch and Papadopoulos's system to clear a specific instance.

23. As per claim 9, Blelloch and Papadopoulos taught the invention substantially as claimed in claims 5-7. Blelloch and Papadopoulos did not specifically teach that wherein each of said task units further comprises two configuration registers CONFIG.L and CONFIG.R which are respectively selected by the binary value of said bit L/R of the control/data register of the instance being considered, the contents of said configuration registers being loaded at the beginning of the algorithm processing for defining the task to be activated, the action to be performed and the instance to be considered. However, Official Notice is taken that both the concept and advantage of using of CONFIG.L and CONFIG.R registers is well known and expected in the art. It would have been obvious to use them to define the tasks that need to be activated. It would have been obvious to use CONFIG.L and CONFIG.R in Blelloch and Papadopoulos' system as the configuration registers to define the tasks, actions and instances.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch and Papadopoulos as applied to claims 1-9 above, and further in view of Fairfield et al (hereinafter Fairfield), US 5,321,842.

25. Fairfield was cited in the previous office action.

26. As per claim 10, Blelloch and Papadopoulos taught the invention substantially as claimed in claims 1-7. Blelloch and Papadopoulos did not specifically teach that wherein said task interconnection logic means is composed of three-state drivers each one of said drivers being associated with one of said tasks as input task and a number of buses equal to the number of said tasks as output tasks, one of said buses being selected by the driver corresponding to an input task after decoding an action word by said driver. However, the use of three-state driver is well known in the art and would have been obvious to implement the task interconnection logic means with three-state drivers. Fairfield taught a processor using three-state drivers (col.2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Papadopoulos and Fairfield because Fairfield's teaching of using three-state drivers help to employ feedback to the processor in Blelloch and Papadopoulos' system.

Response to Arguments

27. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lapourtre et al, US 5,136,708.

Torii, US 6,389,446.

Suzuki, US 4,760,608.

29. A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenny Lin whose telephone number is (703)305-0438. The examiner can normally be reached on 8 AM to 5 PM Tuesday to Friday and every other Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (703)305-8498. Additionally, the fax numbers for Group 2100 are as follows:

Official Responses: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-6121.

ksl
March 24, 2004

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100